Homework 7: 100 Points

This Homework contains examples of multiprocessors and cache coherency.

Please submit your answers in a document and upload it in Canvas by the due date.

Present your work neat, clear, organized, logical, and make your case; don’t leave it to our interpretation of your answer. There is 10% penalty per day for delay in submitting the homework.

1. (25 Points) Using the architecture and data of Chapter 5, Example 5, write the result of the following actions using the method of Example 5. Note that as in Example 5, all these operations are independent of each other and performed on the original state of Memory and Cache.
2. P0: read 120
3. P0: write 120 ← 80
4. P3: write 120 ← 80
5. P1: read 110
6. P0: write 105 ←48
7. P0: write 130 ← 78
8. P3: write 130 ← 78
9. (25 Points) Consider a dual core (A and B) with
   1. Snooping Protocol
   2. Write Invalidate
   3. Write through
   4. Variable x in memory with content 7

Show the activities and cache and memory content as:

* Core B reads x
* Core A reads x
* Core B writes 2 to x
* Core A reads x
* Core B writes 5 to x

1. (25 Points) Consider a dual core (A and B) with
   1. Snooping Protocol
   2. Write Update
   3. Write Back
   4. Variable x in memory with content 8

Show the activities and cache and memory content as:

* Core A reads x
* Core B reads x
* Core A writes 3 to x
* Core A writes 4 to x
* Core B reads x

1. (25 Points) Exercise 5.22 a, b of Textbook